CLAIM STATUS

1-2. (Cancelled)

3. (Currently Amended) A memory module, comprising: ~~The memory module of claim 1, further comprising~~

a memory device;

a connector;

a plurality of lines coupling the memory device and the connector;

termination circuitry coupled to at least a subset of the lines; and

a termination voltage generator adapted to generate a termination voltage signal, the termination circuitry being configured to terminate the subset of the lines using the termination voltage signal.

4. (Original) The memory module of claim 3, wherein the termination circuitry further comprises a pull-up resistor coupled between each of the lines in the subset and the termination voltage generator.

5. (Original) The memory module of claim 3, wherein the termination voltage generator further comprises a voltage regulator.

6. (Original) The memory module of claim 3, wherein the termination voltage generator further comprises a voltage divider.

7. (Original) The memory module of claim 6, wherein the voltage divider further comprises:

a first resistor having a first terminal coupled to a supply voltage source and a second terminal coupled to one of the lines in the subset; and

a second resistor having a first terminal coupled to the second terminal of the first resistor and a second terminal coupled to ground, the termination voltage signal being generated at the connection of the second terminal of the first resistor and the first terminal of the second resistor.

8. (Currently Amended) A memory module, comprising: ~~The memory module of claim 1,~~

a memory device;

a connector;

a plurality of lines coupling the memory device and the connector; and

termination circuitry coupled to at least a subset of the lines including, ~~wherein the termination circuitry further comprises~~ a plurality of voltage dividers coupled to the lines in the subset, each voltage divider comprising:

a first resistor having a first terminal coupled to a supply voltage source and a second terminal coupled to one of the lines in the subset; and

a second resistor having a first terminal coupled to the second terminal of the first resistor and a second terminal coupled to ground, the termination voltage being generated at the connection of the second terminal of the first resistor and the first terminal of the second resistor.

9-10. (Cancelled)

11. (Currently Amended) The memory module of claim [[1]] 3, further comprising enable circuitry coupled to the termination circuitry and being configured to disable the termination circuitry responsive to a termination disable signal.

~~12. (Original) The memory module of claim 11, wherein the enable circuitry further~~ comprises a plurality of switches coupled between the termination circuitry and the lines.

13. (Original) The memory module of claim 11, wherein the termination circuitry further comprises switchable resistors configured to receive the termination disable signal.

14. (Original) The memory module of claim 11, further comprising a switch configured to provide the termination disable signal.

15. (Currently Amended) A memory module, comprising: ~~The memory module of claim 11, further comprising~~

a memory device;

a connector;

a plurality of lines coupling the memory device and the connector;

termination circuitry coupled to at least a subset of the lines;

enable circuitry coupled to the termination circuitry and being configured to disable the termination circuitry responsive to a termination disable signal; and

a jumper configured to provide the termination disable signal.

16. (Original) The memory module of claim 11, further comprising a termination disable signal line coupled to the connector for providing the termination disable signal.

17. (Currently Amended) The memory module of claim [[1]] 3, wherein the connector further comprises an edge connector.

18-20. (Cancelled)

21. (Currently Amended) A system, comprising: ~~The system of claim 19, wherein the memory module further comprises~~

a circuit board including a memory bus and an expansion socket coupled to the memory bus; and

a memory module including:

a memory device;

a connector adapted to interface with the expansion socket;

a plurality of lines coupling the memory device and the connector;

termination circuitry coupled to at least a subset of the lines; and

a termination voltage generator adapted to generate a termination voltage signal, the termination circuitry being configured to terminate the subset of the lines using the termination voltage signal.

22. (Original) The system of claim 21, wherein the termination circuitry further comprises a pull-up resistor coupled between each of the lines in the subset and the termination voltage generator.

23. (Original) The system of claim 21, wherein the termination voltage generator further comprises a voltage regulator.

24. (Original) The system of claim 21, wherein the termination voltage generator further comprises a voltage divider.

25. (Original) The system of claim 24, wherein the voltage divider further comprises:

a first resistor having a first terminal coupled to a supply voltage source and a second terminal coupled to one of the lines in the subset; and

a second resistor having a first terminal coupled to the second terminal of the first resistor and a second terminal coupled to ground, the termination voltage signal being generated at the connection of the second terminal of the first resistor and the first terminal of the second resistor.

26. (Currently Amended) A system, comprising: ~~The system of claim 19, wherein the termination circuitry further comprises~~

a circuit board including a memory bus and an expansion socket coupled to the memory bus; and

a memory module including:

a memory device;

a connector adapted to interface with the expansion socket;

a plurality of lines coupling the memory device and the connector; and

termination circuitry coupled to at least a subset of the lines including a plurality of voltage dividers coupled to the lines in the subset, each voltage divider comprising:

a first resistor having a first terminal coupled to a supply voltage source and a second terminal coupled to one of the lines in the subset; and

a second resistor having a first terminal coupled to the second terminal of the first resistor and a second terminal coupled to ground, the termination voltage signal being generated at the connection of the second terminal of the first resistor and the first terminal of the second resistor.

27-28. (Cancelled)

29. (Currently Amended) The system of claim [[19]] 21, wherein the memory module further comprises enable circuitry coupled to the termination circuitry and being configured to disable the termination circuitry responsive to a termination disable signal.

30. (Original) The system of claim 29, wherein the enable circuitry further comprises a plurality of switches coupled between the termination circuitry and the lines.

31. (Currently Amended) A system, comprising: ~~The system of claim 29, wherein the termination circuitry further comprises~~

a circuit board including a memory bus and an expansion socket coupled to the memory bus; and

a memory module including:

a memory device;

a connector adapted to interface with the expansion socket;

a plurality of lines coupling the memory device and the connector;

termination circuitry coupled to at least a subset of the lines, comprising switchable resistors configure to receive [[the]] a termination disable signal;

enable circuitry coupled to the termination circuitry and being configured to disable the termination circuitry responsive to the termination disable signal.

32. (Original) The system of claim 29, wherein the memory module further comprises a switch configured to provide the termination disable signal.

33. (Currently Amended) A system, comprising: ~~The system of claim 29, wherein the memory module further comprises~~

a circuit board including a memory bus and an expansion socket coupled to the memory bus; and

a memory module including:

a memory device;

a connector adapted to interface with the expansion socket;

a plurality of lines coupling the memory device and the connector;

termination circuitry coupled to at least a subset of the lines;

enable circuitry coupled to the termination circuitry and being configured to disable the termination circuitry responsive to a termination disable signal; and

a jumper configured to provide the termination disable signal.

34. (Original) The system of claim 29, wherein the memory module further comprises a termination disable signal line coupled to the connector for providing the termination disable signal.

35. (Currently Amended) The system of claim [[29]] 21, wherein the connector further comprises an edge connector.

36. (Cancelled)

37. (Currently Amended) A memory module, comprising: ~~The memory module of claim 36, further comprising~~

a memory device;

a connector;

a plurality of lines coupling the memory device and the connector;

a termination voltage line;

a plurality of pull-up resistors coupled between selected lines of the plurality of lines and the termination voltage line; and

a termination voltage generator coupled to the termination voltage line.

38. (Original) The memory module of claim 37, wherein the termination voltage generator further comprises a voltage regulator.

39. (Original) The memory module of claim 37, wherein the termination voltage generator further comprises a voltage divider.

40. (Original) The memory module of claim 39, wherein the voltage divider further comprises:

a first resistor having a first terminal coupled to a supply voltage source and a second terminal coupled to the termination voltage line; and

a second resistor having a first terminal coupled to the second terminal of the first resistor and a second terminal coupled to ground.

41. (Currently Amended) A memory module, comprising: ~~The memory module of claim 36, further comprising~~

a memory device;

a connector;

a plurality of lines coupling the memory device and the connector;

a termination voltage line;

a plurality of pull-up resistors coupled between selected lines of the plurality of lines and the termination voltage line; and

switches coupled between the pull-up resistors and the termination voltage line, the switches being configured to disable the pull-up resistors responsive to a termination disable signal.

42. (Currently Amended) The memory module of claim [[36]] 37, wherein the connector further comprises an edge connector.

43-44. (Cancelled)

45. (Currently Amended) A method for fabricating a memory module, comprising ~~The method of claim 43, further comprising~~:

providing a circuit board having a connector;

mounting a memory device on the circuit board;

coupling the memory devices to the connector using a plurality of lines;

coupling termination circuitry to at least a subset of the lines;

providing a termination voltage generator on the circuit board to generate a termination voltage signal; and

coupling the termination voltage generator to the termination circuitry.

46. (Original) The method of claim 45, wherein providing the termination circuitry further comprises coupling a pull-up resistor between each of the lines in the subset and the termination voltage generator.

47. (Original) The method of claim 45, wherein providing the termination voltage generator further comprises providing a voltage regulator.

48. (Original) The method of claim 45, wherein providing the termination voltage generator further comprises providing a voltage divider.

49. (Original) The method of claim 48, wherein providing the voltage divider further comprises:

coupling a first terminal of a first resistor to a supply voltage source;

coupling a second terminal of the first resistor to one of the lines in the subset; and

coupling a first terminal of a second resistor to the second terminal of the first resistor; and

coupling a second terminal of the second resistor to ground, the termination voltage signal being generated at the connection of the second terminal of the first resistor and the first terminal of the second resistor.

50. (Currently Amended) A method for fabricating a memory module, comprising ~~The method of claim 43, wherein providing the termination circuitry further comprises~~:

providing a circuit board having a connector;

mounting a memory device on the circuit board;

coupling the memory devices to the connector using a plurality of lines;

coupling termination circuitry to at least a subset of the lines, wherein ~~providing~~ coupling the termination circuitry further comprises providing a plurality of voltage dividers coupled to the lines in the subset, each voltage divider comprising a first resistor having a first terminal coupled to a supply voltage source and a second terminal coupled to one of the lines in the subset and a second resistor having a first terminal coupled to the second terminal of the first resistor and a second terminal coupled to ground, [[the]] a termination voltage being generated at the connection of the second terminal of the first resistor and the first terminal of the second resistor.

51-52. (Cancelled)

53. (Currently Amended) The method of claim [[43]] 45, further comprising coupling enable circuitry to the termination circuitry for disabling the termination circuitry responsive to a termination disable signal.

54. (Original) The method of claim 53, wherein providing the enable circuitry further comprises coupling a plurality of switches between the termination circuitry and the lines.

55. (Currently Amended) A method for fabricating a memory module, comprising: ~~The method of claim 53, wherein providing the termination circuitry further comprises~~

providing a circuit board having a connector;

mounting a memory device on the circuit board;

coupling the memory devices to the connector using a plurality of lines;

coupling termination circuitry to at least a subset of the lines, the termination circuitry comprising switchable resistors configured to receive [[the]] a termination disable signal; and

coupling enable circuitry to the termination circuitry for disabling the termination circuitry responsive to a termination disable signal.

56. (Original) The method of claim 53, further comprising providing a switch on the circuit board configured to provide the termination disable signal.

57. (Currently Amended) A method for fabricating a memory module, comprising: ~~The method of claim 53, further comprising~~

providing a circuit board having a connector;

mounting a memory device on the circuit board;

coupling the memory devices to the connector using a plurality of lines;

coupling termination circuitry to at least a subset of the lines;

coupling enable circuitry to the termination circuitry for disabling the termination circuitry responsive to a termination disable signal; and

providing a jumper on the circuit board configured to provide the termination disable signal.

58. (Original) The method of claim 53, further comprising coupling a termination disable signal line to the connector for providing the termination disable signal.

59-61. (Cancelled)